Claims

I claim:

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1. A system for connecting peripheral devices to a computer, comprising:

a host computer system, wherein said host computer system includes a CPU and memory;

a first parallel bus coupled to the host computer system;

a primary bridge coupled to the first parallel bus, wherein said primary bridge includes parallel interface circuitry for interfacing to the first parallel bus;

a second parallel bus located remotely from said host computer system;

one or more peripheral devices coupled to the second parallel bus; and

a secondary bridge coupled to said second parallel bus, wherein said secondary bridge is located remotely from said host computer system, wherein said secondary bridge includes parallel interface circuitry for interfacing to said second parallel bus; and

a serial bus coupled between said primary bridge and said secondary bridge, wherein the serial bus includes a first end and a second end, wherein said first end of said serial bus is coupled to said primary bridge and said second end of said serial bus is coupled to said secondary bridge;

wherein said primary bridge and said secondary bridge are configured to transmit a parallel bus cycle over said serial bus, wherein said parallel bus cycle includes an address phase and a data phase, wherein said address phase includes a command value and an address value, and wherein said data phase includes a first set of byte enable values and a data value;

wherein said primary bridge is configured to receive said parallel bus cycle, wherein said primary bridge is configured to generate a first command packet that corresponds to said address phase, wherein said primary bridge is configured to generate a plurality of data packets that each correspond to said parallel bus cycle, wherein said first command packet includes a second set of byte enable values, and wherein said primary bridge is configured to set said second set of byte enable values to a set of predetermined values prior to generating said plurality of data packets.

2. The system of claim 1, wherein said primary bridge is configured to compare said first set of byte enable values to said set of predetermined values, and wherein said primary bridge is configured to generate a second command packet if said first set of byte enable values differs from said set of predetermined values.

3. The system of claim 2, wherein said primary bridge is configured to store said first set of byte enable values in said second command packet if said first set of byte enable values differs from said set of predetermined values.

4. The system of claim 2, wherein said primary bridge is configured to discard said first command packet if said first set of byte enable values differs from said set of predetermined values.

5. The system of claim 1, wherein said primary bridge is configured to set said second set of byte enable values irrespective of said first set of byte enable values.

6. The system of claim 1, wherein said primary bridge further includes a FIFO queue, wherein said FIFO queue includes a head and a tail, wherein said primary bridge is configured to store said command value and said address value in said FIFO queue upon receipt of said address phase, and wherein said primary bridge is configured to generate said first command packet when said command value reaches said head of said FIFO queue.

7. The system of claim 6, wherein said primary bridge is configured to store said first set of byte enable values and said data value in said FIFO queue upon receipt of said data phase, wherein said primary bridge is configured to compare said first set of byte enable values to said set of predetermined values when said first set of byte enable values reaches said head of said FIFO queue, and wherein said primary bridge is

configured to generate a second command packet if said first set of byte enable values differs from said set of predetermined values.

8. The system of claim 7, wherein said second command packet includes a third set of byte enable values, and wherein said primary bridge is configured to set said third set of byte enable values equal to said first set of byte enable values if said first set of byte enable values differs from said set of predetermined values.

9. The system of claim 1, wherein a first of said plurality of data packets corresponds to said address value, wherein a second of said plurality of data packets corresponds to said data value, and wherein said primary bridge is configured to transmit said first command packet and said plurality of data packets to said secondary bridge over said serial bus.

10. The system of claim 1, wherein said first parallel bus comprises a Peripheral Component Interconnect (PCI) bus, and wherein said second parallel bus comprises a Peripheral Component Interconnect (PCI) bus.

11. A method for for transmitting a parallel bus cycle over a serial bus in a computer system, the method comprising:

generating said parallel bus cycle in a host computer, wherein said parallel bus cycle includes an address phase and a data phase, wherein said address phase includes a command value and an address value, and wherein said data phase includes a first set of byte enable values and a data value;

transmitting said parallel bus cycle from said host computer to a primary bridge over a first parallel bus;

generating a first command packet in said primary bridge, wherein said first command packet includes a second set of byte enable values, and wherein said first command packet corresponds to said address phase of said parallel bus cycle; and

generating a plurality of data packets in said primary bridge, wherein each of said plurality of data packets corresponds to said parallel bus cycle;

wherein said generating said first command packet includes setting said second set of byte enable values to a set of predetermined values prior to generating said plurality of data packets.

12. The method of claim 11, further comprising:

comparing said first set of byte enable values to said set of predetermined values in said primary bridge; and

generating a second command packet in said primary bridge if said first set of byte enable values differs from said set of predetermined values, wherein said second command packet includes said first set of byte enable values.

13. The method of claim 12, further comprising:

discarding said first command packet in said primary bridge if said first set of byte enable values differs from said set of predetermined values.

14. The method of claim 11, further comprising:

transmitting information from said primary bridge to a secondary bridge over a serial bus;

recreating said parallel bus cycle in said secondary bridge in response to receiving said information from said primary bridge;

transmitting said parallel bus cycle from said secondary bridge to a peripheral device over a second parallel bus;

comparing said first set of byte enable values to said set of predetermined values in said primary bridge; and

generating a second command packet in said primary bridge if said first set of byte enable values differs from said set of predetermined values.

15. The method of claim14, wherein said second command packet includes a third set of byte enable values, wherein said generating said second command packet includes setting said third set of byte enable values equal to said first set of byte enable values if said first set of byte enable values differs from said set of predetermined values, and wherein said transmitting said information includes transmitting said second command packet and said plurality of data packets if said first set of byte enable values differs from said set of predetermined values.

16. The method of claim 11, wherein said setting said second set of byte enable values includes setting said second set of byte enable values to said set of predetermined values irrespective of said first set of byte enable values.

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17. The method of claim 11, further comprising:

storing said command value and said address value in a FIFO queue in said primary bridge upon receipt of said address phase; and

performing said generating said first command packet when said address phase reaches a head of said FIFO queue.

18. The method of claim 17, further comprising:

storing said first set of byte enable values and said data value in said FIFO queue in said primary bridge upon receipt of said data phase;

comparing said first set of byte enable values to said set of predetermined values when said first set of byte enable values reaches said head of said FIFO queue; and

generating a second command packet in said primary bridge if said first set of byte enable values differs from said set of predetermined values.

19. The method of claim 18, wherein said second command packet includes a third set of byte enable values, wherein said generating said second command packet includes setting said third set of byte enable values equal to said first set of byte enable values if said first set of byte enable values differs from said set of predetermined values,

and wherein said transmitting said information includes transmitting said second command packet and said plurality of data packets if said first set of byte enable values differs from said set of predetermined values.

20. The method of claim 11, wherein a first of said plurality of data packets corresponds to said address value, wherein a second of said plurality of data packets corresponds to said data value, and wherein said transmitting said information includes transmitting said first command packet and said plurality of data packets.

21. The method of claim 11, wherein said first parallel bus comprises a Peripheral Component Interconnect (PCI) bus, and wherein said second parallel bus comprises a Peripheral Component Interconnect (PCI) bus.

22. A bus bridge configured to transmit a parallel bus cycle over a serial bus in a computer system, wherein said bus bridge is configured to receive said parallel bus cycle, wherein said parallel bus cycle includes an address phase and a data phase, wherein said address phase includes a command value and an address value, and wherein said data phase includes a first set of byte enable values and a data value, comprising:

a queue configured to store said address phase and said data phase;

a transmitter pipeline coupled to said queue, wherein said transmitter pipeline is configured to generate a first command packet in response to an address phase reaching a head of said queue, wherein said first command packet includes a second set of byte enable values, and wherein said transmitter pipeline is configured to set said second set of byte enable values to a set of predetermined values prior to said data phase reaching said head of said queue; and

a transmitter coupled to said transmitter pipeline, wherein said transmitter is configured to transmit a plurality of packets over said serial bus in a serial format.

23. The bus bridge of claim 22, wherein said transmitter pipeline is configured to compare said first set of byte enable values to said set of predetermined values when

said data phase reaches said head of said queue, and wherein said transmitter pipeline is configured to generate a second command packet if said first set of byte enable values differs from said set of predetermined values.

24. The bus bridge of claim 23, wherein said transmitter pipeline is configured to store said first set of byte enable values in said second command packet if said first set of byte enable values differs from said set of predetermined values.

25. The bus bridge of claim 24, wherein said transmitter pipeline is configured to generate a first data packet corresponding to said address value stored in said queue, wherein said transmitter pipeline is configured to generate a second data packet corresponding to said data value stored in said queue, and wherein said transmitter is configured to transmit said second command packet, said first data packet, and said second data packet if said first set of byte enable values differs from said set of predetermined values.

26. The bus bridge of claim 25, wherein said transmitter is configured to transmit said first command packet, said first data packet, and said second data packet if said first set of byte enable values does not differ from said set of predetermined values.

27. The bus bridge of claim 23, wherein said transmitter pipeline is configured to discard said first command packet if said first set of byte enable values differs from said set of predetermined values.

28. The bus bridge of claim 22, wherein said transmitter pipeline is configured to set said second set of byte enable values irrespective of said first set of byte enable values.

29. The bus bridge of claim 22, wherein said queue includes a FIFO queue.

30. The bus bridge of claim 22, wherein said transmitter pipeline is configured to generate a first data packet corresponding to said address value stored in said queue, wherein said transmitter pipeline is configured to generate a second data packet corresponding to said data value stored in said queue, and wherein said transmitter is configured to transmit said first command packet, said first data packet, and said second data packet.

31. The bus bridge of claim 22, wherein said bus bridge comprises a PCI bus bridge.

32. A method for transmitting a parallel bus cycle over a serial bus in a computer system, the method comprising:

generating said parallel bus cycle in a host computer, wherein said parallel bus cycle includes a first phase and a second phase;

transmitting said parallel bus cycle from said host computer to a first bridge over a first parallel bus;

generating a first packet in said first bridge, wherein said first packet includes a set of predicted values that correspond to said second phase of said parallel bus cycle, and wherein said first packet corresponds to said first phase of said parallel bus cycle; and

generating a second packet in said first bridge, wherein each of said plurality of data packets corresponds to said parallel bus cycle;

wherein said generating said first packet includes setting said set of predicted values to a set of predetermined values prior to generating said second packet.

33. The method of claim 32, further comprising:

transmitting information from said first bridge to a second bridge over a serial bus;

recreating said parallel bus cycle in said second bridge in response to receiving said information from said first bridge; and

transmitting said parallel bus cycle from said second bridge to a peripheral device over a second parallel bus.

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